What Goes In The Library?

(What should the SCA Require to Document a Waveform?)

JTRS JPO FPGA/DSP Workshop

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A Comprehensive List of Waveform Documentation - Requirements to be Met by Documentation

- Unambiguous
- Understandable by others not involved in the development
- Hierarchy shows top down design from system to SW component level and the interconnections of the components

Additional Requirements

- Traceability from models to implementation

The List of Documents

- a) Executable Specification
  - matlab/simulink model or C or C++ model, or industry prefered choices
- b) Networking specification (C language,Opnet, Qualnet, MATLAB, etc
- c) behavioral functional model (state diagrams, block diagrams, refere to the virtual socket interface alliance)
- d) reference implementation (executable model implementation)
- e) test harness and test vectors to validate the models to the implementation
  - bit exact testing
  - Validation test vectors for every API
  - test criteria for floating point)
- f) timing information

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g) Data flow
  - Control flow and Signal Flow at SW FW HW perspectives
- h) other documentation
  - porting strategy document
  - test documents
  - waveform requirements documents
  - SDD
  - traceability of how are all the components trace back to the MATLAB model
- i) waveform control
  - composition (from high level down to discrete devices and constraints)
  - waveform mode controls from external GUI waveform management

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- Source code:
- i) golden waveform
- j) ported waveform
- k) VHDL models
- l) nonrepudiated checksum
- m) error handling
- n) interfaces to smart antenna & other RF externals